IN THE CLAIMS

Please amend claims 1, 9, and 17 as follows:

1. (Currently Amended) A method, comprising:

at least one counter with at least one physical register, wherein said at least one physical register is mapped to a logical register;

updating said at least one counter when one or more instructions are mapped to said logical register;

releasing said at least one physical register based on a value of said at least one counter and after retiring a corresponding checkpoint, irrespective of a commit status of a corresponding instruction as indicated by a re-order buffer.

2. (Original) The method of claim 1, said updating said at least one counter further comprising:

incrementing said at least one counter when at least one instruction with said logical register as an input operand is renamed to said at least one physical register.

3. (Original) The method of claim 2, said updating said at least one counter further comprising:

decrementing said at least one counter when said instruction is issued and reads said at least one physical register.

4. (Original) The method of claim 1, said releasing said at least one physical register further comprising:

releasing said at least one physical register when said counter is decremented, wherein said decrementing reaches a state indicating that none of said instructions have yet to read said at least one physical register.

5. (Cancelled)

6. (Original) The method of claim 1, wherein said checkpoint includes at least one unmapped flag for each of said at least one physical register associated with said checkpoint.

7. (Original) The method of claim 1, wherein said at least one counter is incremented when said checkpoint is generated.

8. (Original) The method of claim 1, wherein said at least one counter is decremented when said checkpoint is retired.

9. (Currently Amended) An apparatus, comprising:

a branch predictor to generate a checkpoint, wherein said checkpoint is associated with at least one physical register;

a checkpoint buffer to maintain said at least one physical register, said at least one physical register associated with one or more instructions;

wherein said branch predictor releases said at least one physical register based on a value of at least one counter that is associated with said at least one physical register and after said checkpoint is released, irrespective of a commit status of a corresponding instruction as indicated by a re-order buffer.

10. (Previously Presented) The apparatus of claim 9, wherein said checkpoint buffer increments said at least one counter when said checkpoint is generated.

11. (Previously Presented) The apparatus of claim 9, wherein said checkpoint buffer decrements said at least one counter when said checkpoint is retired.

12. (Previously Presented) The apparatus of claim 9, wherein said branch predictor increments said at least one counter when at least one of said one or more instructions with a logical register as an input operand is renamed to said at least one physical register.

13. (Previously Presented) The apparatus of claim 9, wherein said branch predictor decrements said at least one counter when at least one of said one or more instructions is issued and reads said at least one physical register.

14. (Previously Presented) The apparatus of claim 9, wherein said branch predictor releases said at least one physical register when said at least one counter is decremented to a state indicating that none of said one or more instructions have yet to read said at least one physical register.

15. (Cancelled)

16. (Original) The apparatus of claim 9, wherein said checkpoint includes at least one unmapped flag for each of said at least one physical registers associated with said checkpoint.

17. (Currently Amended) A system, comprising:

a processor including a branch predictor to [[to]] generate a checkpoint, wherein said checkpoint is associated with at least one physical register, a checkpoint buffer to maintain said at least one physical register, said at least one physical register associated

with one or more instructions, wherein said branch predictor releases said at least one physical register based on a value of at least one counter that is associated with said at least one physical register and after said checkpoint is retired, irrespective of a commit status of a corresponding instruction as indicated by a re-order buffer;

an interface to couple said processor to input-output devices; and

a data storage coupled to said interface to receive code from said processor.

18. (Previously Presented) The system of claim 17, wherein said checkpoint buffer increments said at least one counter when said checkpoint is generated.

19. (Previously Presented) The system of claim 17, wherein said checkpoint buffer decrements said at least one counter when said checkpoint is retired.

20. (Previously Presented) The system of claim 17, wherein said branch predictor increments said at least one counter when at least one of said one or more instructions with a logical register as an input operand is renamed to said at least one physical register.

21. (Previously Presented) The system of claim 17, wherein said branch predictor decrements said at least one counter when at least one of said one or more instructions is issued and reads said at least one physical register.

22. (Previously Presented) The system of claim 17, wherein said branch predictor releases said at least one physical register when said at least one counter is decremented to a state indicating that none of said one or more instructions have yet to read said at least one physical register.

23. (Cancelled)

24. (Original) The system of claim 17, wherein said checkpoint includes at least one unmapped flag for each of said at least one physical registers associated with said checkpoint.

25. (Original) The method of claim 1, further comprising releasing said checkpoint after all instructions associated with said checkpoint have completely executed.

26. (Original) The system of claim 9, wherein said branch predictor retires said checkpoint after all instructions associated with said checkpoint have completely executed.

27. (Original) The system of claim 17, wherein said branch predictor releases said checkpoint after all instructions associated with said checkpoint have completely executed.